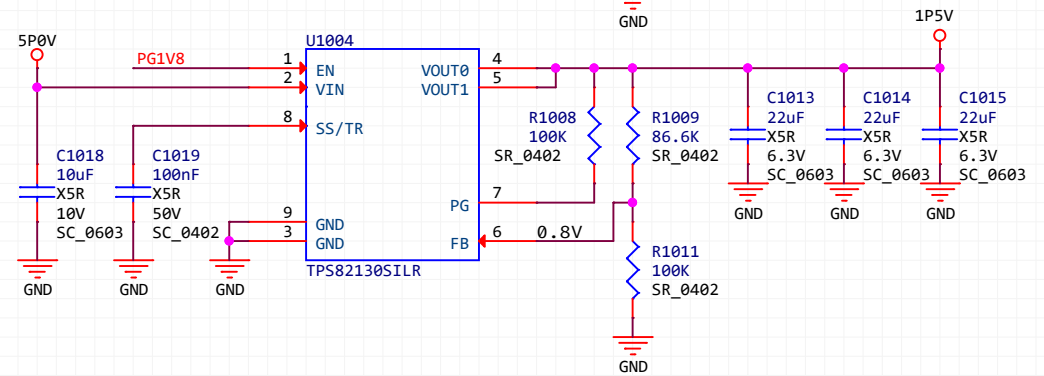
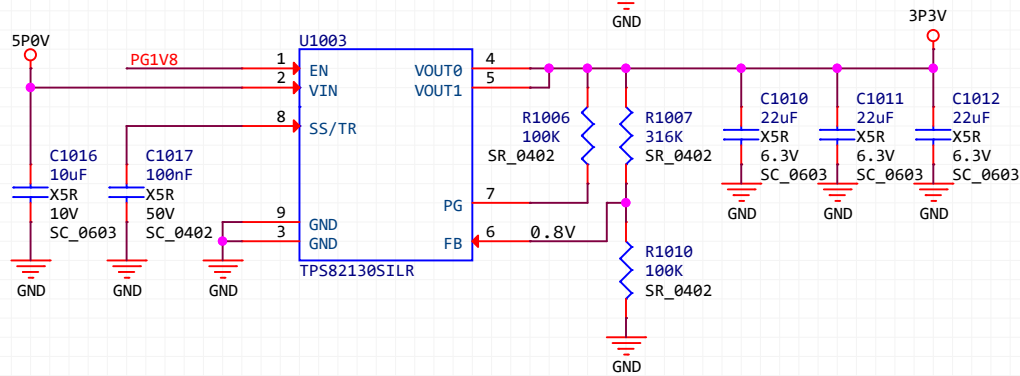
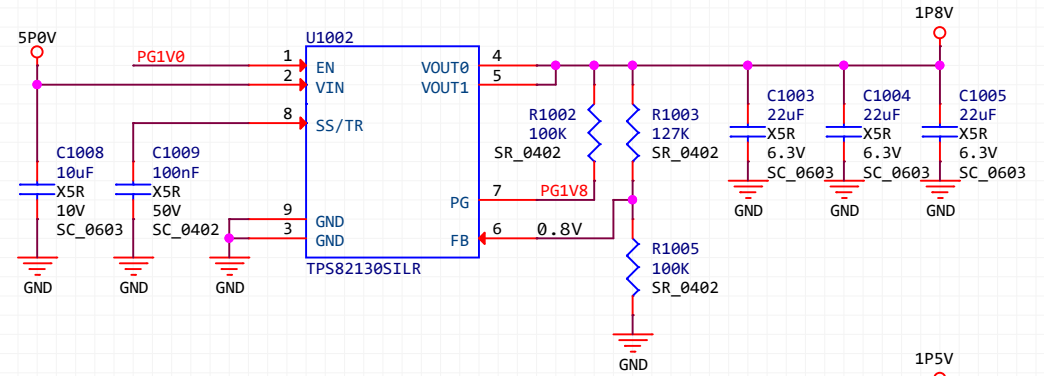
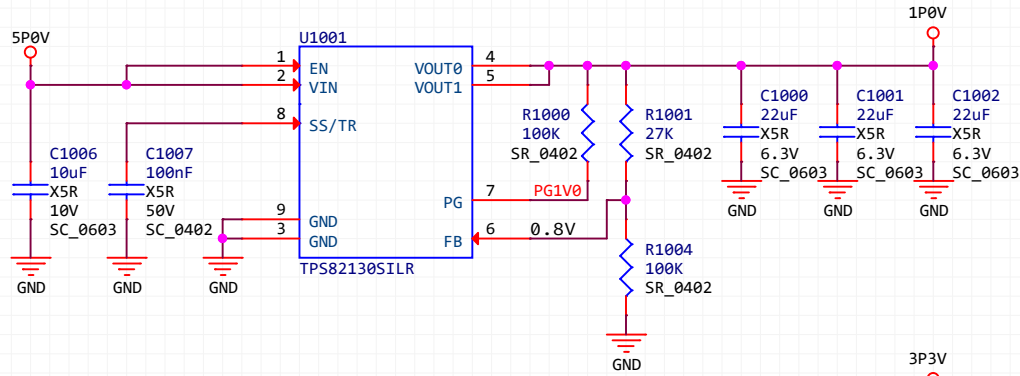
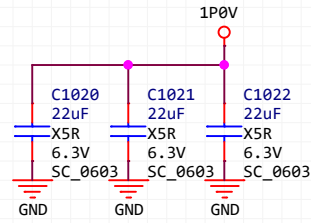
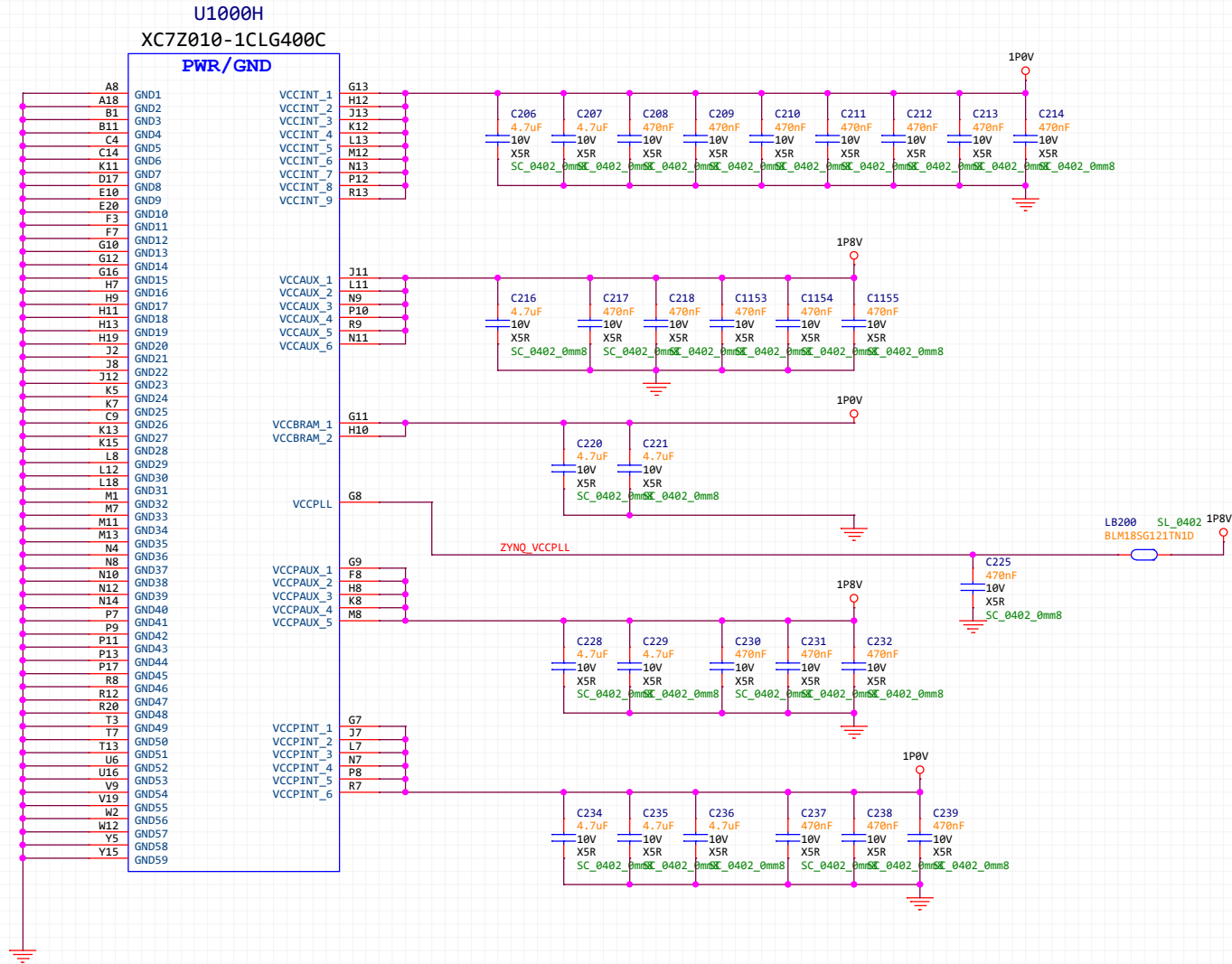


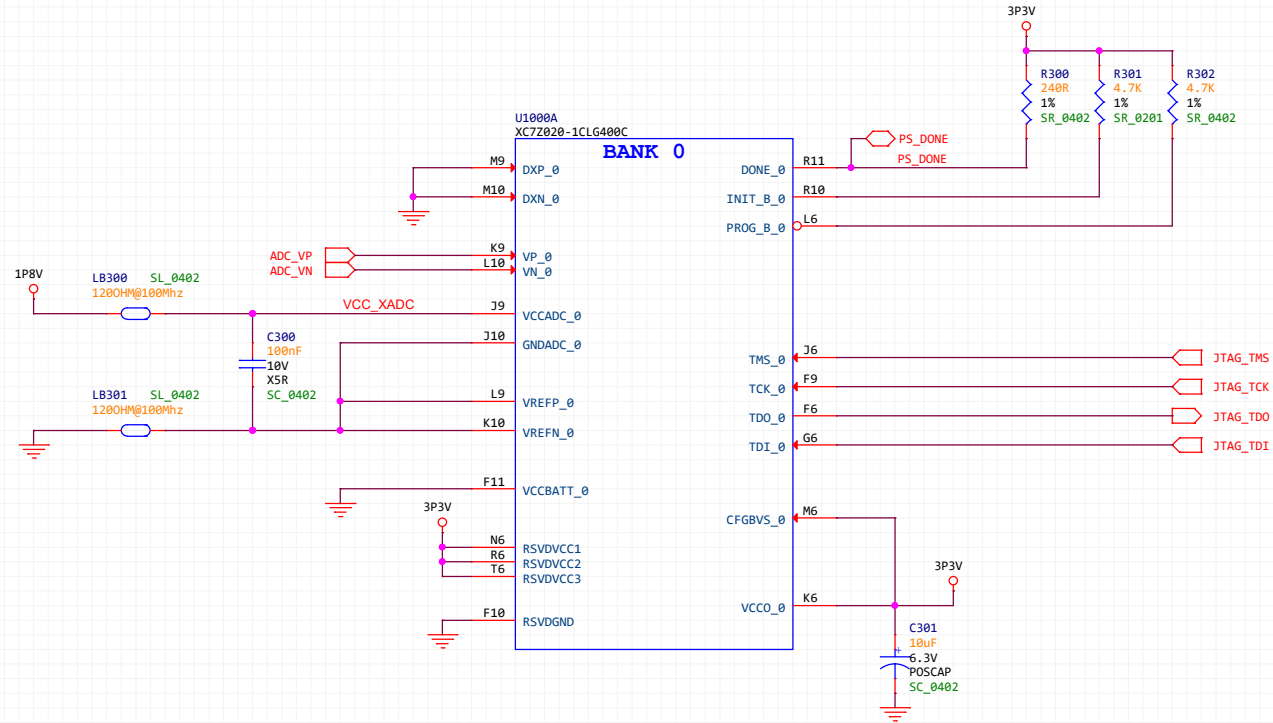
POWER



ZYNQ POWER

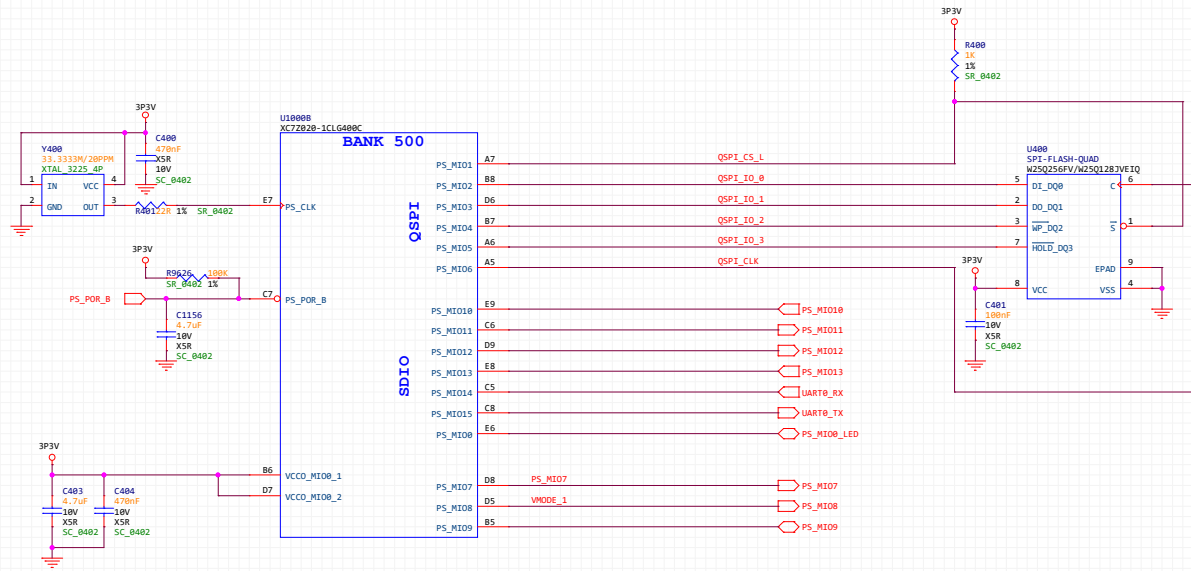


ZYNQ BANK 0



BANK 0 OPERATING VOLTAGE = 3.3V

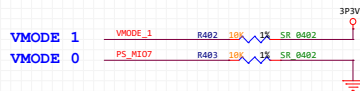
ZYNQ BANK500



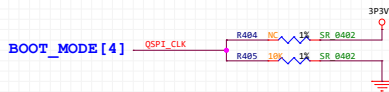
ZYNQ CONFIG MODE SELECT

Layout Note:

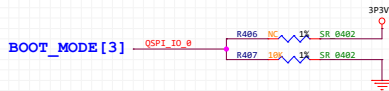
Limit the Stub length to less than 10mm



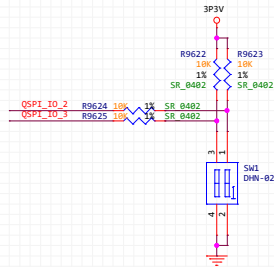
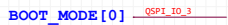
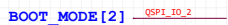
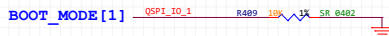
VMODE 1 = 1 -----> MIO Bank 1 Voltage = 1.8V
VMODE 0 = 0 -----> MIO Bank 0 Voltage = 3.3V



BOOT_MODE4 = 1 -----> PLL Bypassed
BOOT_MODE4 = 0 -----> PLL Used

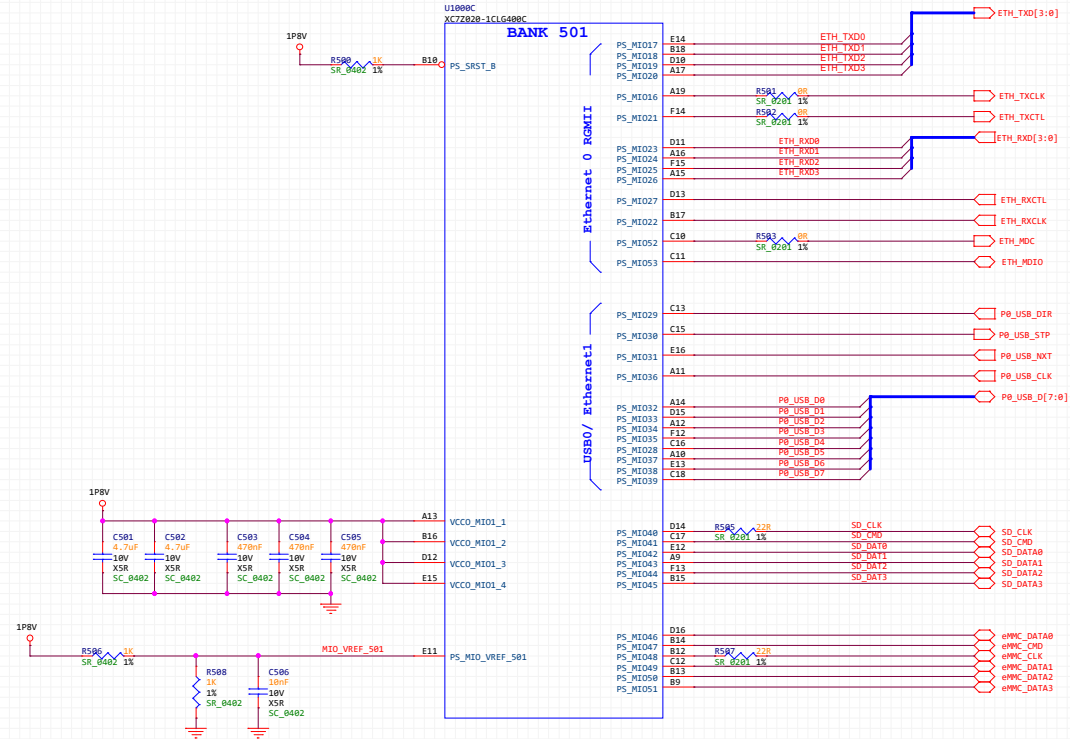


BOOT_MODE3 = 1 -----> Independant JTAG
BOOT_MODE3 = 0 -----> Cascaded JTAG



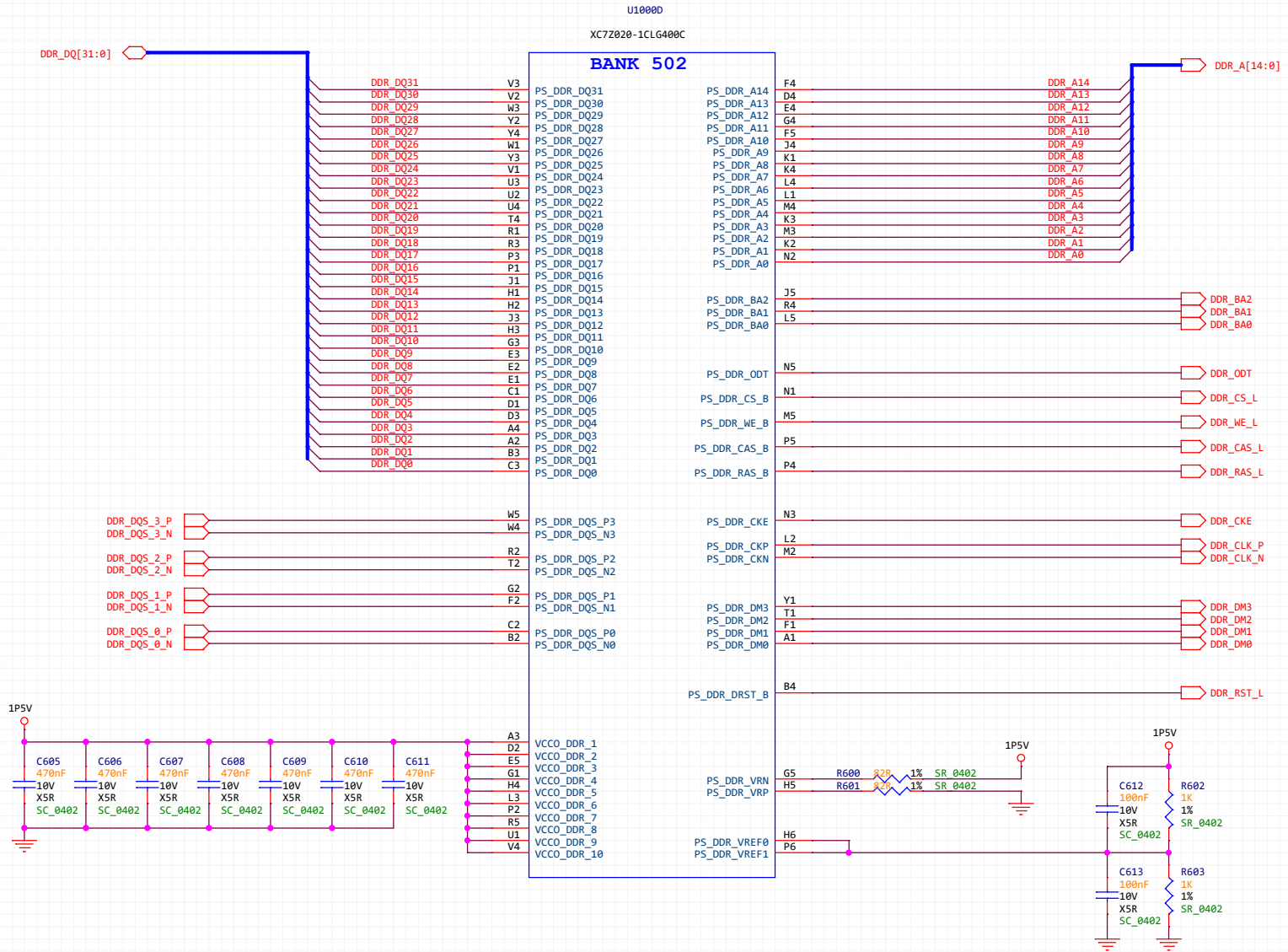
BOOT_MODE[0]	BOOT_MODE[1]	BOOT_MODE[2]	BOOT_MODE[3]	
0	0	0	0	Boot from JTAG
1	0	0	x	Boot from QSPI

ZYNQ BANK501



1.8V Interface IO

ZYNQ BANK502

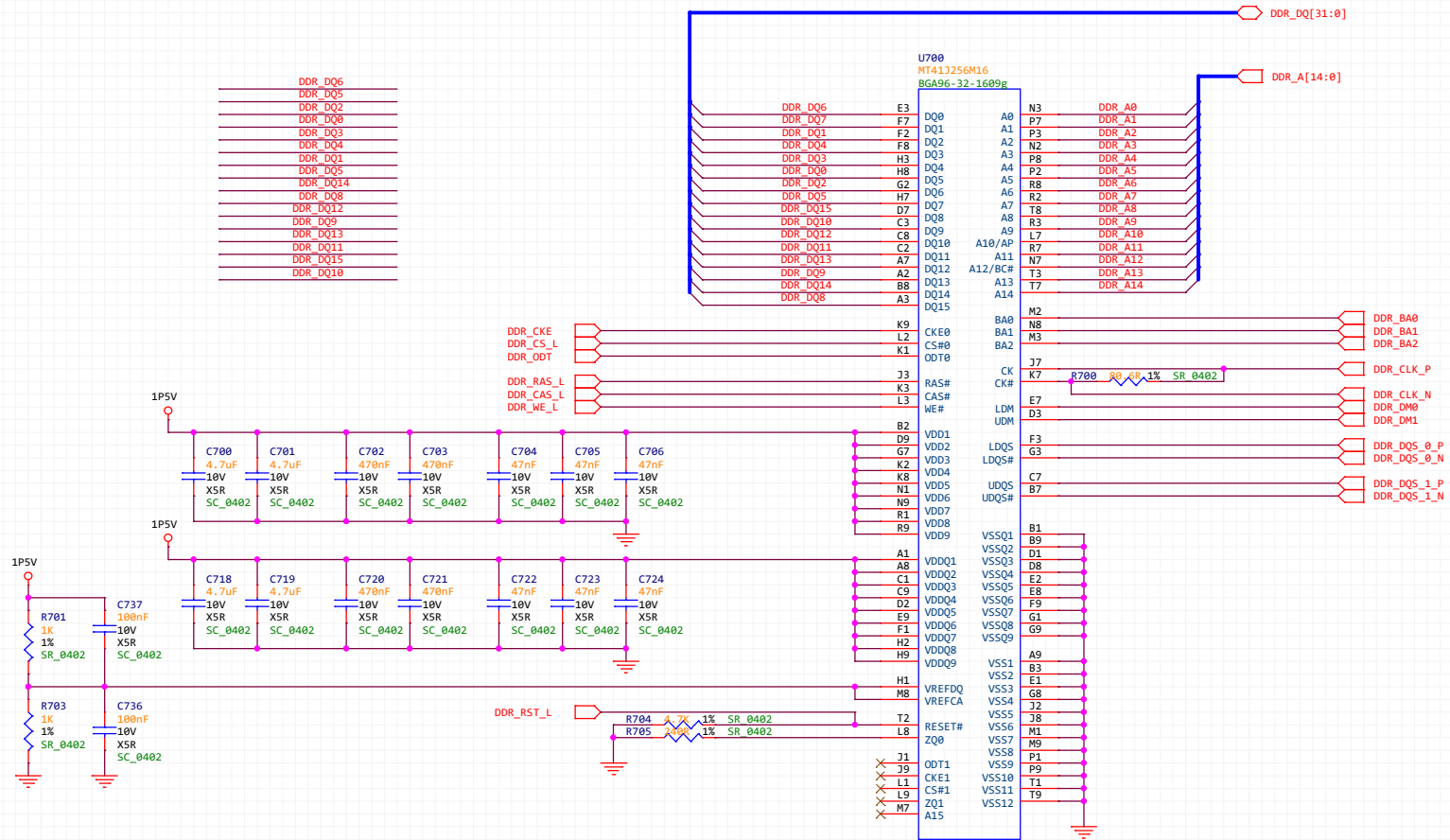


ZYNQ BANK34&35

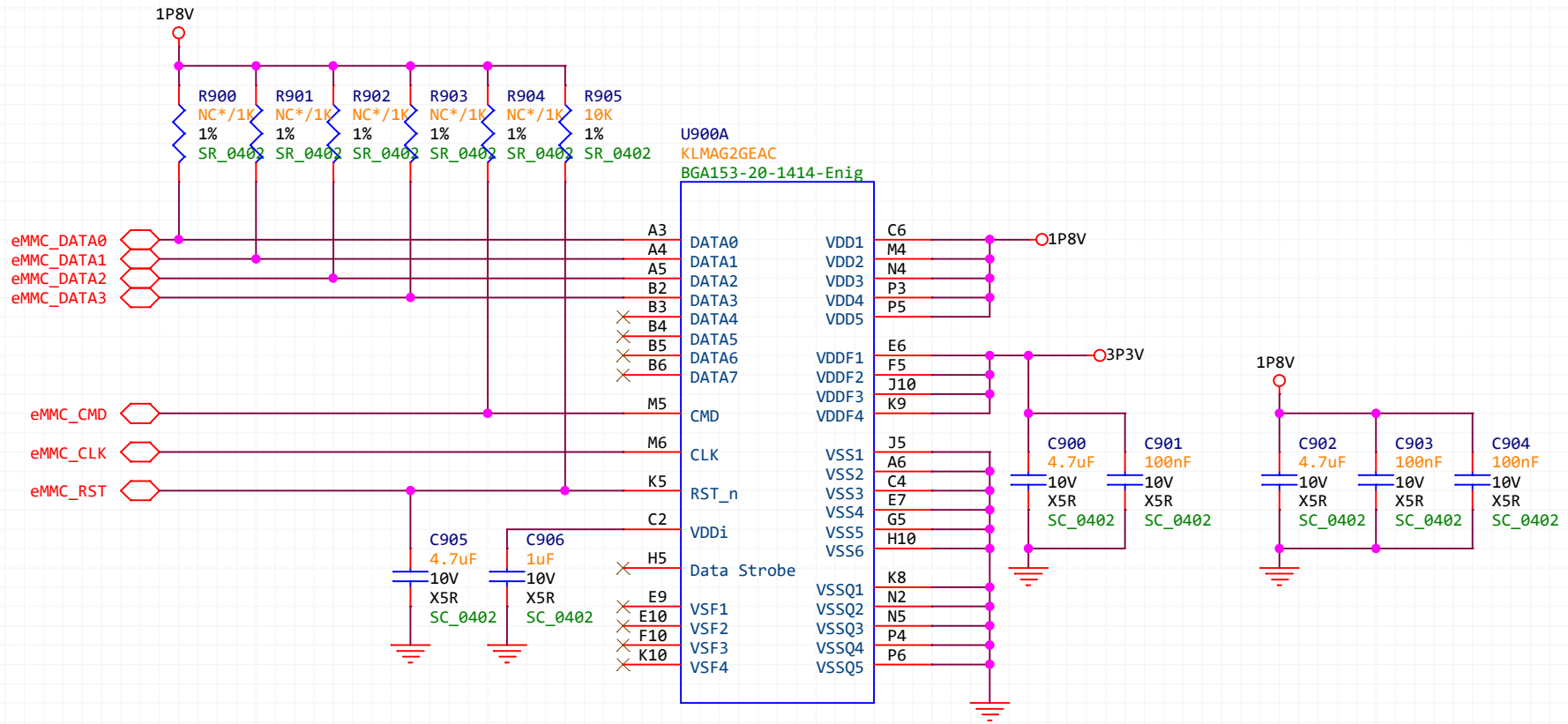
Enable 100-ohm internal termination on all LVDS inputs



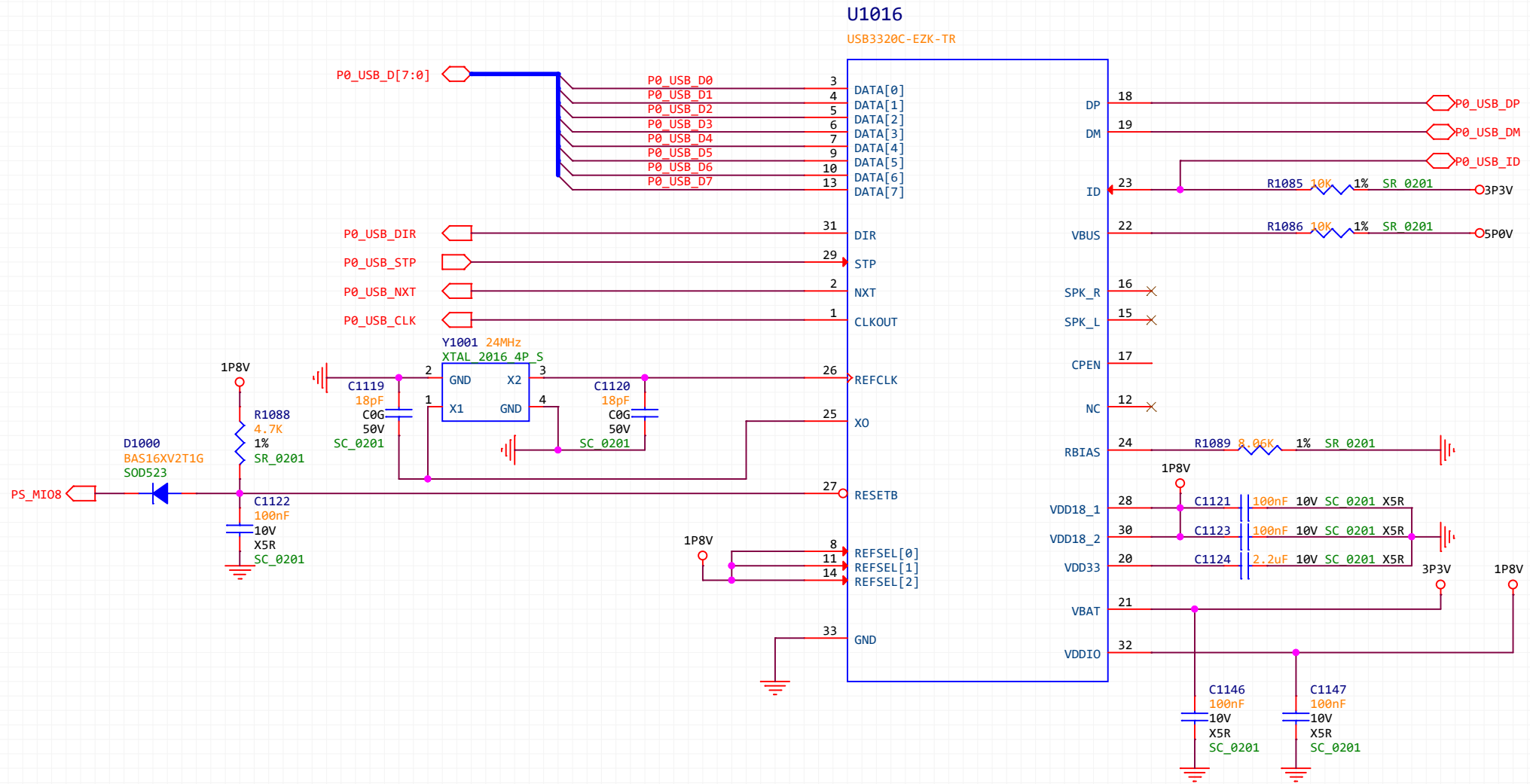
DDR3



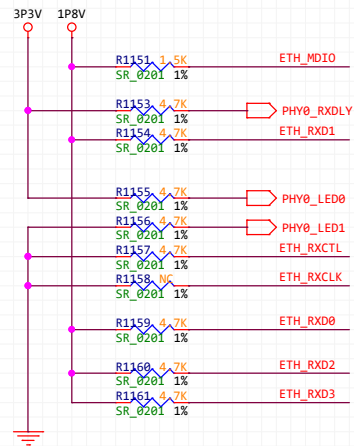
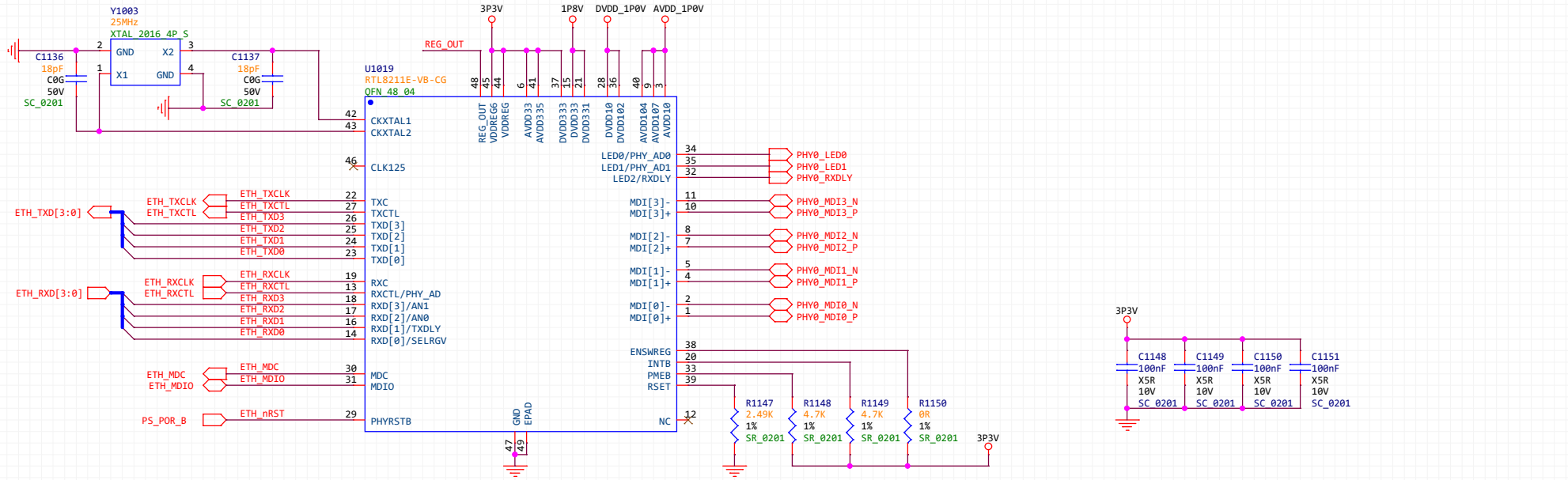
eMMC



USB PHY



ETH PHY

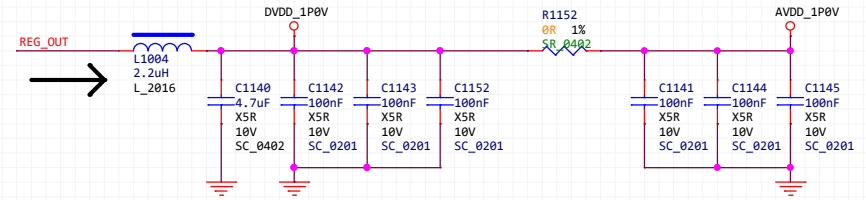


RGMII clock timing control

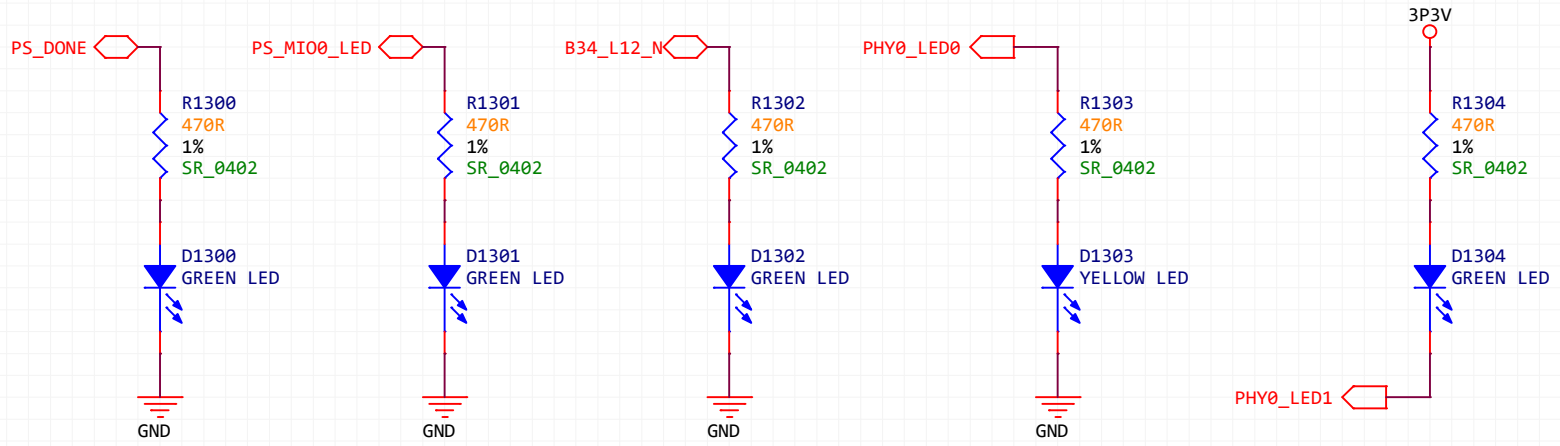
PHY Address is 0x01

Pull up for RGMII 1.8V

Nway, Advertise all capabilities



LED



Connector

